ABSTRACT

The present invention is a computer memory error management system and method that facilitates fault tolerant memory I/O in a manner that permits smooth and continuous operations. The system and method handles memory control buffer corruption concerns associated with memory errors and corrects single bit errors. Information is placed in a memory controller buffer and a determination is made if a correctable error or non-correctable error exists in the information. If the error is a correctable error it is corrected in-line. A memory cell error resolution process is performed and information is rewritten to a memory control buffer location. If rewriting to the same memory controller buffer location does not solve the error, a hard error handling process is performed. A hard error handling process and a non-correctable error handling process utilize a fail over process in which an alternate memory controller performs the I/O operations.